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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,938	12/03/2003	Holger Hoppe	543822002400	4491

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EXAMINER	
NGUYEN, VINH P	
ART UNIT	**PAPER NUMBER**
2829	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/28/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/725,938	HOPPE, HOLGER	
	Examiner	Art Unit	
	VINH P. NGUYEN	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. The proposed drawing correction filed on 10/18/2006 is acceptable.

2. Claims 7,13,16,18,20-22 are objected to because of the following informalities:

In claim 7, it is unclear how the testing time frame is determined less than 2 second after loading of the carrier with the semiconductor chip. Which device is used for determing this testing time frame.

In claim 13, it is still unclear what " a loading chip" comprises of. Is it shown in any of drawings? Is this loading chip the same as "the semiconductor chip"?

. Appropriate correction is required.

In claim 16,18,20-22,it appears that the limitation of "used for testing the functioning of the semiconductor chip" and "used during ordinary operation of the semiconductor chip" would not further limit the scope of the invention but it is considered as intended use and this limitation is not given any patentable weights.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-24,26,28-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsuda (Pat # 4,730,156).

As to claims 1,12-13,26,28-29, Matsuda discloses in figure # 2 an apparatus for testing contacting between a semiconductor chip and a carrier having a carrier (16a,16b,16c,16d) for

coupling to a semiconductor chip (10a,10b,10c,10d) and a plurality of contacting test contacts (162a,162b,162c,162d) for exclusively testing the contacting between the semiconductor chip and the carrier (16a,16b,16c,16d). It is noted that the carrier (16a,16b,16c,16d) is considered as a "test carrier" since it is connected to a detection circuit (30,32,34,36) and the semiconductor chip is directly contacted with the contacts (14) of the test carrier (16a,16,16c,16d).

As to claims 2 and 14, it appears that the carrier (162a,162b,162c,162d) electrically coupled to a testing apparatus (30,34,32,36).

As to claim 3, it appears that the carrier is connected to the testing apparatus and the carrier (16a,16b,16c,16d) is subsequently loaded with semiconductor chip (10a,10b,10c,10d).

As to claim 4, it appears that the carrier (16a,16b,16c,16d) is inherently loaded at a carrier loading station and the contacting between the carrier and the semiconductor chip is tested before the carrier is transported to a further station after all tests are done.

As to claim 5 , the contacting between the carrier and the chip is tested by the testing apparatus (30,32,34,36).

As to claim 6, the device of Matsuda is configured to test the contacting between the carrier and the semiconductor chip but not functioning of the chip.

As to claim 7, performing the contacting between the carrier and the semiconductor chip being tested by the testing apparatus (34,30,32,36) less than 2 seconds after loading of the carrier with the chip is considered as an inherent function of the testing apparatus (30,32,34 and 36).

As to claims 8-9, the contacting testing between the carrier and the chip is determined whether an electric contact has been established between a corresponding pad (104a,106a,104b,106b,104c,106c,104d,106d) and the assigned pads (162a,164a,162b,164b,162c,164c,162d,164d) of the carrier (16a,16b,16c,16d).

As to claim 10, it appears that there is a current flowing through the corresponding chip pad to the testing apparatus (30,34,32,36) in order to trigger the indicator (36) for indicating the electric contact between the chip and the carrier.

As to claim 11, when the contact between the semiconductor chip and the carrier is properly connected, the indicator (36) is lit up, that means there is an amount of voltage dropping across the chip pad and that voltage is determined by the indicator (36).

As to claims 15 and 19, it appears that some of the contacting test contacts (see figure 2 , test contacts on the upper left corner of the chip (10a,10b,10c,10d) are not used during ordinary operation of the chip.

As to claims 16,18,20-22, Matsuda also disclose additional contact (104 or 106).

As to claims 17 and 21, the contacts (104a, 106a,104b,106b,104c,106c,104d,106d) are not used for testing the functioning of the chip during contacting test between the semiconductor chip and the carrier.

As to claims 23-24, Matsuda discloses one or more contacting test contacts (104a,106a,104b,106b,104c,106c,104d,106d) are provided on a bottom of the chip (10a,10b,10c,10d).

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 25 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuda (Pat # 4,730,156) in view of Farnworth (Pat # 6,369,595).

As to claims 25 and 27, Matsuda et al disclose an apparatus for testing contacting between a semiconductor chip and a carrier. However, the carrier (16a,16b,16c,16d) of Matsuda et al is not a TSOP test carrier.

Farnworth et al teach that it would have been well known to have the TSOP socket (31) (see column 8, lines 6-8).

It would have been obvious for one of ordinary skill in the art to consider that the carrier (16a,16b,16c,16d) of Matsuda et al is a TSOP test carrier as taught by Farnworth et al since this type of the socket is well known in the art for supporting a certain IC package.

7. Applicant's arguments with respect to claims 1-24 have been considered but are moot in view of the new ground(s) of rejection.

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tran (pat # 6,472,891) disclose method and apparatus for testing semiconductor packages without damage.

Ellwood et al (Pat # 3,573,617) disclose method and apparatus for testing packaged integrated circuit.

Kang (pat # 6,323,669) discloses apparatus and method for a contact test between an integrated circuit device and a socket.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VINH P. NGUYEN whose telephone number is 571-272-1964. The examiner can normally be reached on 6:30AM-4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, HA T. NGUYEN can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

VINH P NGUYEN
Primary Examiner
Art Unit 2829
12/20/06